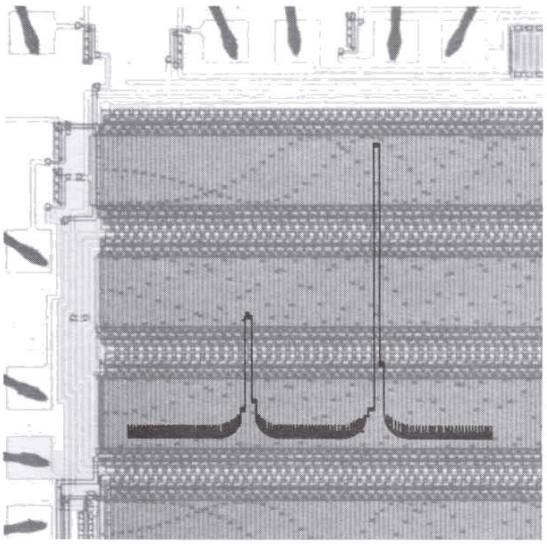
RETICON® PRODUCT SUMMARY: DISCRETE TIME ANALOG SIGNAL PROCESSING DEVICES

Reticon offers a broad line of integrated circuits which can be used to perform analog signal processing functions. All of these devices function in the discrete-time domain by storing samples of the input signal in an analog memory as packets of charge. These analog samples are then manipulated to produce such operations as delay, multiplication and addition. This results in devices which can perform such functions as frequency changing, filtering, correlation, and Fourier transforming.

There are two basic categories of devices based on the way in which the analog samples are handled. In the *Charge Transfer Devices* **(CTD)** each sample of charge is transferred from stage to stage across the chip under the control of a sequence of clock pulses. There are two types of these multiple transfer devices, *Bucket Brigade Devices* **(BBD)** and *Charge Coupled Devices* **(CCD)**. The differences between them are primarily in the details of the device structure. From the functional point of view BBD's offer a way to make practical tapped analog delay lines for such applications as correlators and externally programmable transversal filters. The CCD technology is capable of higher sampling rates and higher density devices. These include such devices as the video delay and the 512 point transversal filters.

The second major category is *Single Transfer Devices* **(STD)**. These devices are similar to an integrated set of multiplexed sample-and-holds. Each successive sample is stored in a separate discrete memory cell, where it stays until it is read out. These devices have applications as video delays, data buffers, and time base correctors. They don't have the problem of transfer inefficiency of CTD's because of the single transfer but have performance limitations associated with fixed-pattern and clocking noise.



Photomicrograph of quad CCD filter R5601-2 used to produce the power spectrum density of two sine waves at 10 and 20 KHz shown superimposed on the integrated circuit.

CHARGE TRANSFER DEVICES (CTD)

The concept of a CTD is to store a sample of analog information as a packet of charge on a capacitor and then under the control of a clock to transfer it to the next storage site. A simple analogy can be made to a two-phase water bucket-brigade shown in Figure 1.

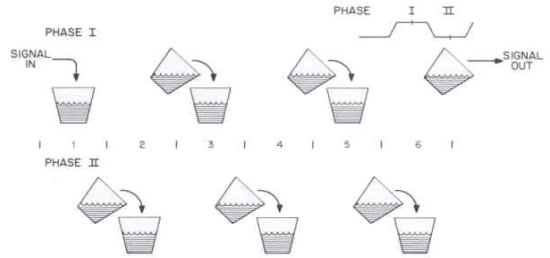


Figure 1. Analogy of Charge Transfer Device

From this simple model, several device features can be seen. First, since in one phase the input is being filled and in the other it is being transferred, the device is sampling the input data signal. If nothing is done at the output, the signal is present for a half clock cycle and the other half cycle the output comes to a reference level.

The key parameter for a CTD is the transfer inefficiency (ϵ). The charge transfer inefficiency is the fraction of charge left behind on each transfer. If one bucket containing 10,000 electrons is dumped into the next bucket, and it leaves behind a single electron, then $\epsilon = 1 \times 10^{-4}$. Since the same fraction is left behind each time a transfer is made then for an entire device the total inefficiency in $n\epsilon$, where n is the number of transfers. The effect of this on a sine wave input is similar to that of a low pass filter. The quantitative results are the amplitude attenuation:

$$Aout/Ain = \exp\,[-n\epsilon(1-\cos 2\pi\, f/f_c)]$$

where f is the input frequency (always less than the Nyquist frequency, $f_c/2$) and f_c is the sample rate. The additional phase delay over the expected ideal value is:

$$\Delta\phi = n\epsilon \sin(2\pi\, f/f_c)\ .$$

The transfer inefficiency is determined by device parameters which determine the time required for the charge to transfer from one bucket to the next. If the clock frequency is continually increased, a point is reached where insufficient time is allowed for all the charge to transfer.

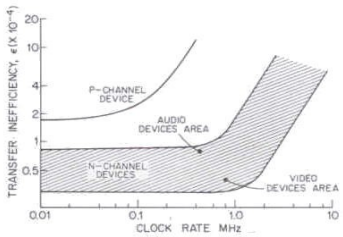


Figure 2. Charge transfer inefficiency versus clock frequency

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Figure 2 shows how ϵ behaves as a function of the clock frequency for Reticon n-channel BBD devices. Note the higher frequency response relative to a p-channel device which has lower mobility and hence lower transfer efficiency.

The following is a summary and functional description of Reticon CTD devices now available or in development.

SUMMARY OF CHARGE TRANSFER DEVICES (CTD)

Part No.	Description	Number of Samples Stored	Max Sample Rate	Analog Sig. Bandwidth (6db down)	Signal / Noise	Clock Drive	Pkg (Pins)	Evaluation Circuit
BUCKET-BRIGADE DEVICE								
SAD-1024A	Dual 512 Stage Audio Delay	512	1 MHz	200 KHz	70 db	2 Ø	16	SC-1024A
SAD-512	512 Stage Audio Delay	256	1 MHz	200 KHz	70 db	2 Ø	16	SC-1024A
SAD-512D	512 Stage Audio Delay with Driver	256		200 KHz	70 db	1 Ø	8	SC-512D
TAD-32A	32 Stage Tapped Delay	32	5 MHz	2 MHz	70 db	2 Ø	40	TC-32A(1)
R5401	64 Sample Binary Analog Correlator	64	10 MHz			2 Ø	16	RC5401
NEW **R5501**	32 Parallel Inputs/Serial Output	32	5 MHz	2 MHz	60-80(2)	2 Ø	40	RC5501
R5602	Family of Transversal Filters	64					16	
CHARGE COUPLED DEVICE								
R5101	2000 Sample Audio Delay	2000	1 MHz	200 KHz	80 db	1 Ø	22	RC5101
R5102	455 Sample Video Delay	455	16 MHz	(2)	70 db	4 Ø	16	RC5102
R5103	910 Sample Video Delay	910	16 MHz	(2)	70 db	4 Ø	16	RC5102
R5601	Quad Chirped Transversal Filter	1024	2 MHz		70 db	4 Ø	22	RC5601

Notes:

(1) Three versions available. Specify desired type by dash number -01 has fixed tap weight resistors, -02 adjustable taps using potentiometers and -03 without resistors.

(2) Depends on operating conditions. See individual data sheet.

I. BUCKET BRIGADE DEVICES (BBD)

All Reticon BBD devices use n-channel, silicon gate technology with a tetrode gate. The input structure is a NMOS transistor switch which connects the analog signal to the input capacitor (See Figure 3). The charge stored on this capacitance is then transferred from bucket to bucket by the input clocks. The output signal is obtained from a source follower at the end of the line or from a source follower at each stage as in the TAD-32A (See Figure 3B). The device input signal usually consists of a band limited analog signal, which varies around a DC bias level. This composite signal then meets the requirement that the input is always positive with respect to common. The output, likewise, has the analog signal riding on a DC pedestal.

(3A)

(3B)

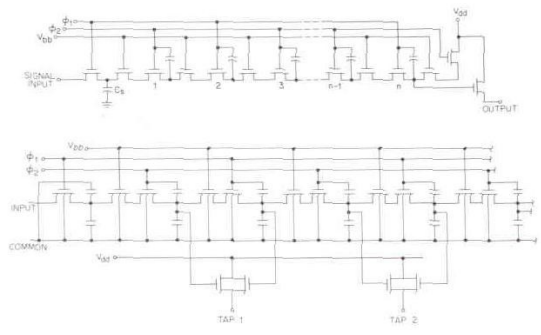

Figure 3. BBD Structure

1. SAD-1024A Serial Analog Delay

The SAD-1024A is a dual 512 stage (256 sample) audio delay line. It has excellent performance characteristics, with better than 70 db dynamic range when measured with a 1 KHz bandwidth and less than 1% distortion. Each section is independent and has two stages per sample stored.

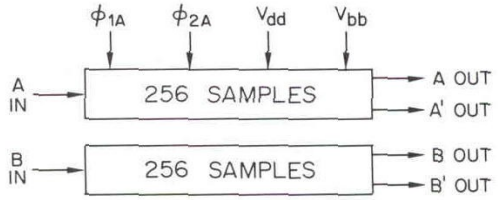

Figure 4. Block Diagram of SAD-1024A

Delay time through each half is equal to 256 divided by the sample frequency with a minimum of 256 μsec and a maximum of about a 100 milliseconds at room temperature. The signal bandwidth is equal to one-half the sample frequency, but has a maximum of 200 KHz. Operation can also be by serial connection, parallel-multiplex or by differential operation of the two sections. Various musical effects such as vibrato or flanging can be achieved by feedback and clock modulation. The SAD-1024A is also used in such applications as data compression and as a voice actuated switch.

2. SAD-512 Serial Analog Delay

The SAD-512 is identical to one section of a SAD-1024A. It contains only one 512 stage (256 sample) delay section. It is useful where only one section is needed or even the slightest crosstalk between sections of a common package would be objectionable.

3. SAD-512D Serial Analog Delay with Driver

The SAD-512D is similar to the SAD-512 except that it contains an on-chip clock driver and thus requires only a single phase, 5 volt clock input. It is intended for high volume low-cost applications but where performance is still important. It is capable of sample rates up to 1 MHz, a dynamic range of 70 db and a throughput gain of approximately unity. It has similar applications to the SAD-1024A and SAD-512.

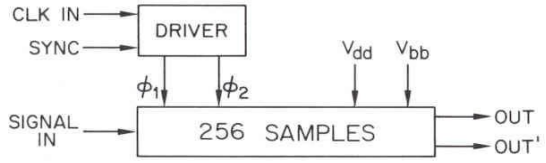

Figure 5. Block Diagram of SAD-512D

4. TAD-32A Tapped Analog Delay

The TAD-32A is a thirty-two stage delay line with an output at each stage. The outputs come from two source followers, one from each element of the stage (see Figure 3B) to give a full wave output with reduced clock modulation. Each tapped output is delayed one sample time from the preceding one. In addition, there is a feedforward output to allow multiple devices to be cascaded. Many signal processing applications are possible with the most obvious being transversal filters, recursive filters and correlators. When used as a transversal filter (no feedback) external resistors are connected to the outputs to form the tap weight function. The TAD-32A is capable of sampling rates from 1 KHz to 5 MHz and dynamic ranges greater than 60 db. The new "A" version reduces the odd-even pattern in the output of the original TAD-32.

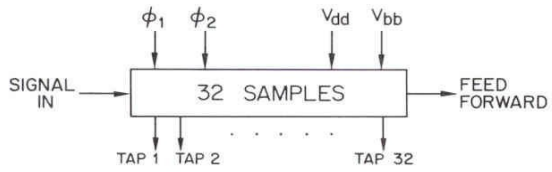

Figure 6. Block Diagram of TAD-32A

5. R5401 Binary to Analog Correlator

The R5401 is a BBD device which performs correlation between a programmable binary function and an analog input signal. The binary values multiply the analog signal in a p-n fashion and the positive and negative products are summed into two common lines which are processed by an off-chip amplifier. The analog signal is internally multiplexed between two 32 stage tapped delay lines. The analog samples are then switched to either a positive or negative output line depending on the content of the static binary registers. Each binary shift register can be programmed with 32 different bits by a 5 volt clock at rates up to 1 MHz. The analog signal can be sampled at up to 10 MHz rates. Typical applications are processing gain in radars using Barker or Pseudo-random codes, and spread spectrum for anti-jamming communications.

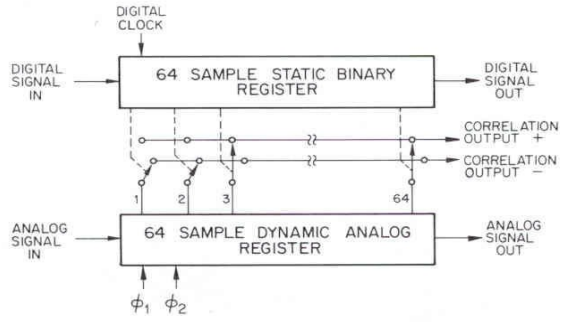

Figure 7. Functional Diagram of R5401 Binary to Analog Correlator

6. R5602 Transversal Filter

The R5602 mask programmed filters are a family of 64 stage BBD devices available with various filter functions. It is intended that these filters will be used for high volume applications and also in those specialized applications which require their unique features. In general, these filters can be made with linear phase and with skirts greater than 100 db/octave. These will operate to sampling rates of 1 MHz and have ultimate rejection in the stopband of typically 50 db. The end of the pass band for low pass filters and the center frequency for band pass filters will be a function of the input clock. Varying the clock frequency gives easily tuneable filter characteristics.

Transversal filters are formed by using split electrodes to form capacitors whose size is related to the desired tap weight function. As the sampled signal moves down the line, it induces current in these capacitors which is proportional to the product of the tap weight and the signal amplitude. All the signals from each half of the electrodes are summed together and then both sides are subtracted in a differential amplifier. The weighting functions are programmed onto the device during fabrication by a pattern on the processing mask. A standard family of low pass, band pass, and chirped filters will be available. In addition, custom devices can be designed to meet individual requirements. Calculated tap weights for custom devices can be checked out using the TAD-32A. This is analogous to verifying digital codes in PROM before committing them to a mask programmable ROM.

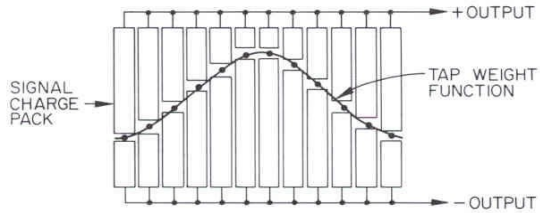

Figure 8. Conceptual Diagram of a Split Electrode Structure

II. CHARGE COUPLED DEVICES (CCD)

The basic principle of the charge coupled device involves the storing of mobile minority charge carriers in a depletion region under a pulsed electrode. When the device has a set of electrodes which are periodically interconnected, the charge can be moved under the direction of the applied clocks. The

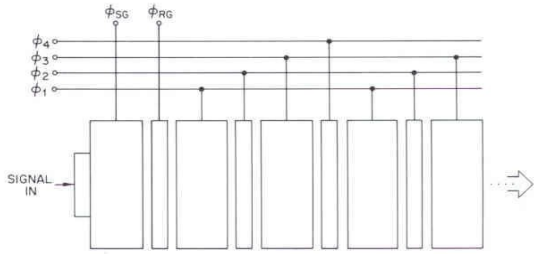

Figure 9. Basic Structure of CCD

clocks cause the array of potential wells to overlap and move with the charge flowing to the deepest well, or the place of lowest energy. Reticon's CCD devices are made using an n-channel, four-phase structure. The clocks are either externally generated or derived from an on-chip driver depending

on the device. The analog input signal rides on a DC bias level to assure that the input is always positive with respect to common.

1. R5101 2000 Sample Serial Analog Delay

The R5101 is a 2000 stage audio delay line with on-chip drivers to simplify its use. Applications include musical effects, medical, geophysical and seismic instrumentation. The device has two outputs, one delayed an additional half sample time to provide a full wave output. There is also a sync input to the driver which allows several devices to be cascaded. The single phase clock input (CLK) can accept any voltage from TTL levels up to the V_{dd} supply. The R5101 has very good performance with an 80 db dynamic range and less than 1% harmonic distortion in narrow band applications. It is capable of sampling frequencies from 1 KHz to 1 MHz.

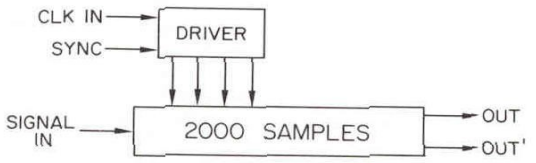

Figure 10. Block Diagram of R5101

2. R5103 910 Sample Video Delay

The R5103 is a serial video delay line capable of sampling rates to 16 MHz. When sampled at 14.318 MHz the delay is equal to one horizontal line time for NTSC television. For TV applications the R5103 can be used for time base correction and drop out compensation. Although designed with television applications in mind, it will find many applications in a wide variety of signal processing functions where high sampling rates are required. Such applications are signal enhancement and data buffering for use in radar, sonar, instrumentation and medical electronics.

The basic structure consists of two delay lines internally multiplexed. Dynamic range is better than 50 db for a 3 MHz bandwidth with harmonic distortion more than 40 db down.

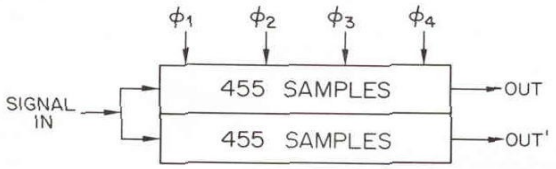

Figure 11. Block Diagram of R5103

02 455 Sample Video Delay

The R5102 is similar to the R5103 except that it has half as many stages. When used in TV applications it has 31.8 usec of delay, or one half of a horizontal TV line. Structure and performance is the same as the R5103.

i Chirped Transversal Filter

The R5601 performs the convolution portion of the chirp Z algorithm to perform either a Discrete Fourier Transform or the power spectral density of the input signal. The basic algorithm requires the input signal to be multiplied by a linear FM signal (a chirp), then to convolve that product with another chirp waveform and finally to post multiply the output with the same FM waveform of the pre-multiplier. There are then two outputs, the real and the imaginary parts.

Two device types are available; the R5601-1 which has the linear chirped waveforms and the R5601-2 with this function multiplied by a Hanning window function. The R5601-1 can do either the total DFT or the power spectral density while the R5601-2 can only do the power spectral density. Each of the R5601 devices contains four 512-tap split electrode transversal filters, two sine and two cosine chirps. The device takes in 512 time samples and outputs 512 coefficients. It is capable of sampling the input signal at rates up to 2 MHz. Figure 12 shows the block diagram of the power spectral density function and the dotted portion indicates the function contained on the device. Reticon also has circuit boards which perform the entire function.

Our RC5601-2 board can operate to 100 KHz and has an output signal-to-noise in excess of 70 db. Applications are numerous as the Fourier transform is a basic tool for signal processing. Some application areas are in voice analysis, bandwidth compression, vibration analysis, instrumentation, radar and communications.

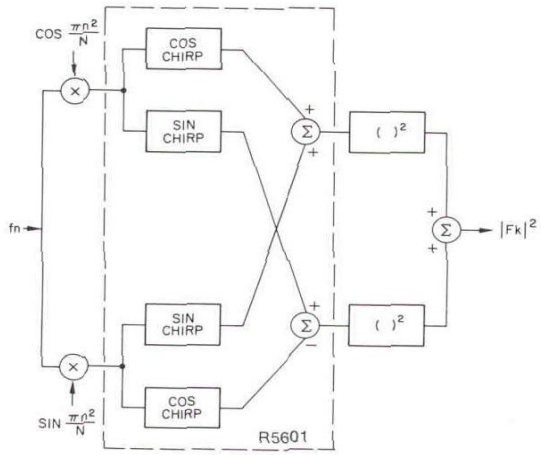

Figure 12. Block Diagram of CZT Algorithm

SINGLE TRANSFER DEVICES (STD)

This family of devices uses standard MOS device structures, such as transistors and capacitors to implement analog functions.

These devices are essentially a set of N parallel integrated sample-and-holds (see Figure 13). The switches are MOS transistors and the capacitors are back biased p-n junctions. The switches are turned on and off by a bit in the shift register, which is also integrated on the chip. The shift register can contain all zeros in which case no switches are closed, or it can contain a single logical one. The bit position determines which switch is closed. The bit is either externally loaded, as in the SAM-64 or internally generated, as in the SAD-100. The maximum sampling frequency is determined by how fast the register can be made to run. The low frequency limit is determined by the leakage current from the back biased diode which is also adding charge to the storage site. The effect of the leakage is dependent on both the storage time and the device temperature. At room temperature the integrated leakage current is about 1% of the storage capacity at a 50 millisecond storage time (except for the long retention SAM-128LR). The leakage doubles for every 7°C rise in temperature and decreases by half for every 7° of cooling.

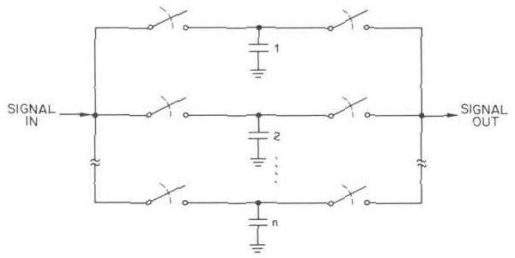

Figure 13. Sample-and-Hold Model of Single Transfer Devices

The following table is a summary of Reticon's standard STD devices.

		Serial Analog Memory	Serial Analog Delay	Serial Analog Memory
		SAM-64	SAD-100	SAM-128LR
Maximum Sample Rate (f_S)		12 MHz	12 MHz	1 MHz
Typ Retention Time (1% Loss, 25°C, See Note 5)		40 ms	40 ms	5 sec.
Analog Signal Bandwidth (Single Pole 6 db)		6 MHz	6 MHz	500 KHz
Signal/Noise		50 db	60 db	70 db
Aperture Time Jitter		< 5 ns	< 5 ns	< 5 ns
Acquisition Time (-4V to +4V)		25 ns	25 ns	800 ns
Readout		Destructive	Destructive	Destructive
Drive Requirements	Clock In	2Ø	4Ø	2Ø
	Clock Out	2Ø	None	2Ø
	Start In	Yes	None	Yes
	Start Out	Yes	None	Yes
	Other		Reset	Reset
Distortion (Total Harmonic)		1%	1%	1%
Delay Bandwidth Product		> 10^4	49	> 10^5
Delay IN-OUT *(Sample Periods)*		1 to 63	98	127
Package		16 pin DIP	16 pin DIP	16 pin DIP
Evaluation Circuit		SC64	SC100	SC128LR

1. SAM-64 Serial Analog Memory

The SAM-64 contains 64 memory cells and independent read-in and read-out shift registers. Sample rates of 5KHz to 12MHz are possible with corresponding but variable delays of up to 5μsec at 12 MHz sample rate and up to 13msec at 5KHz sample rate. Dynamic range is approximately 55db or more. Particular applications are time-base modification or correction of analog signals through the video range. The high speed, wide dynamic range, and independent control of readout of the SAM-64 are particularly advantageous in such applications.

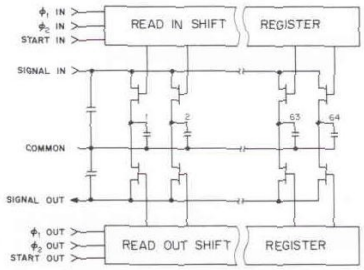

Figure 14. Simple Equivalent Circuit of the SAM-64

2. SAM-128LR Serial Analog Memory

The SAM-128LR is similar in function to the SAM-64 with the exceptions that it has 128 memory cells and the structure is modified to permit very long retention times – up to 5 seconds or more at room temperature, and even longer at reduced temperatures.

Two outputs are provided, one odd, one even. Odd memory cells are multiplexed to the odd read-out line; even memory cells are multiplexed to the even readout line. Internal shunt switches permit operation in an output sample-and-hold configuration for enhanced performance at long delay times. Sample rates as low as 10Hz and as high as 1MHz are possible. Corresponding delay is as much as five seconds at 10Hz sample rate and up to 125μsec at 1MHz. Dynamic range is in excess of 70db, and distortion typically less than 1%. This device is particularly useful in sonar, geophysical, and other low-frequency signal-processing applications.

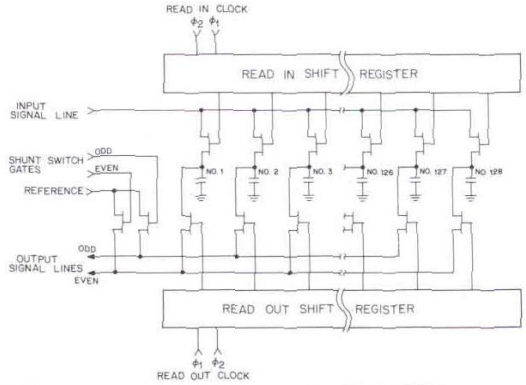

Figure 15. Simple Equivalent Circuit of the SAM-128LR

3. SAD-100 Serial Analog Delay

The SAD-100 is a simplified memory device for use where only delay is desired. It is organized as two delay sections of fifty elements each, featuring sampling rates up to 12MHz with the sections parallel-multiplex connected. Delay (multiplexed) of $98/f_{sample}$ seconds, and 66db dynamic range is available. The SAD-100, with its high speed, wide dynamic range and simplified driving requirements, is particularly useful in those applications where non-dispersive clock-controlled delay is desired.

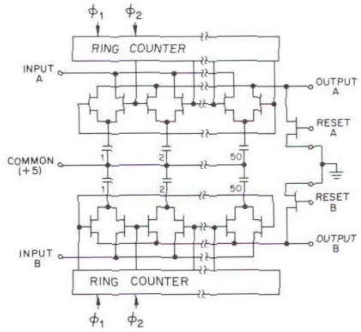

Figure 16. Simple Equivalent Circuit of the SAD-100